Tutorial AN4 (BJT amplifiers)

1. For the common-emitter amplifier in Fig. 1, let V_{CC} = 9 V, R_1 = 27 kΩ, R_2 = 15 kΩ, R_E = 1,2kΩ, and R_C = 2,2 kΩ. The transistor has β = 100 and V_A = 100 V. Assume "mid-band" operation i.e. C_1, C_2, $C_E \rightarrow \infty$

Calculate the dc bias currents I_E and I_C. Is the BJT in the active region? If the amplifier operates between a source with R_{sig} = 10 kΩ and a load R_L = 2 kΩ, draw a small-signal equivalent circuit using a π-model for the BJT, and find the values of R_{in}, the voltage gains $A_v \equiv v_o/v_{in}$ and $A_{v\,sig} \equiv v_o/v_{sig}$ and the current gain $A_i \equiv i_L/i_{in}$.

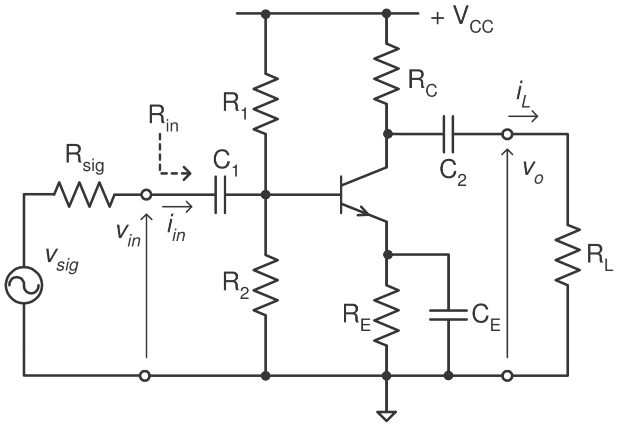

Figure 1

[$I_E = 1{,}94\,\text{mA}$; $A_v = -78{,}85\,\text{V/V}$; $A_{v\,sig} = -8{,}13\,\text{V/V}$; $A_i = -45{,}3\,\text{A/A}$]

2. A designer, having examined the situation described in Q1 and estimating the available gain $A_{v\,sig}$ to be approximately −8 V/V, wishes to explore the possibility of improvement by reducing the loading of the source by the amplifier input. As an experiment, the designer varies the resistance levels by a factor of approximately 3: R_1 to 82 kΩ, R_2 to 47 kΩ, R_E to 3,6 kΩ, and R_C to 6,8 kΩ. With dc supply voltage, source and load values unchanged, what does the gain become? Comment on the result.

[$A_v = -10{,}1\,\text{V/V}$]

3. The amplifier of Fig. 2 consists of two identical common-emitter amplifiers connected in cascade. Observe that the input resistance of the second stage, R_{in2}, constitutes the load resistance of the first stage.

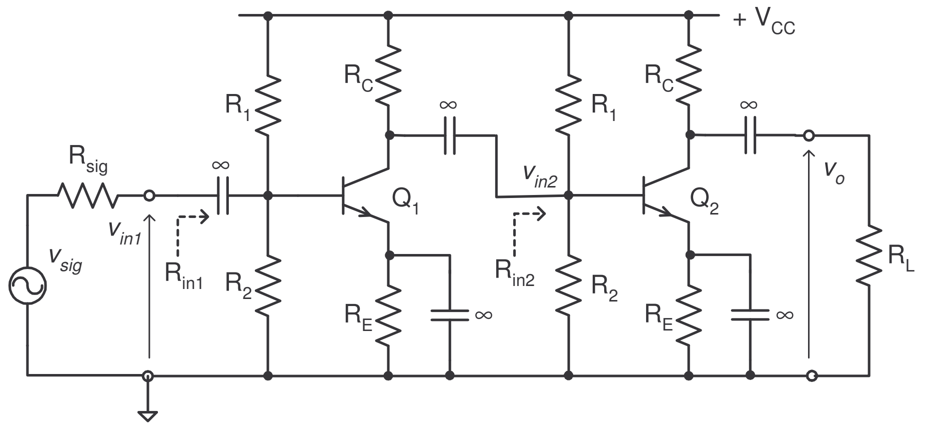

Figure 2

3.1 For V_{CC} = 15 V, R_1 = 100 kΩ, R_2 = 47 kΩ, R_E = 3,9 kΩ, R_C = 6,8 kΩ, and β = 100, determine the dc collector current and collector voltage of each transistor.

3.2 Draw the small-signal equivalent circuit of the entire amplifier and give the values of all its components. Neglect r_{o1} and r_{o2} and assume mid-band operation.

3.3 Find R_{in1} and v_{in1}/v_{sig} for R_{sig} = 5 kΩ.

3.4 Find R_{in2} and $A_{v1} \equiv v_{in2}/v_{in1}$

3.5 For R_L = 2 kΩ, find $A_{v2} \equiv v_o/v_{in2}$

3.6 Find the overall voltage gain $A_{v\,sig} \equiv v_o/v_{sig}$

[$I_C = 0{,}96\,\text{mA}$; $R_{in1} = 2{,}4\,\text{k}\Omega$; $R_{in2} = 2{,}4\,\text{k}\Omega$; $A_{v1} = -68{,}1\,\text{V/V}$; $A_{v2} = -59{,}3\,\text{V/V}$; $A_{v\,sig} = 1292\,\text{V/V}$]

4.1 For the BJT amplifier circuit in Fig. 3, determine the BJT node voltages and V_{CE}, and the currents I_E and I_C in the BJT assuming for the silicon BJT: $V_{BE} = 0,7$ V and $\beta = 150$.

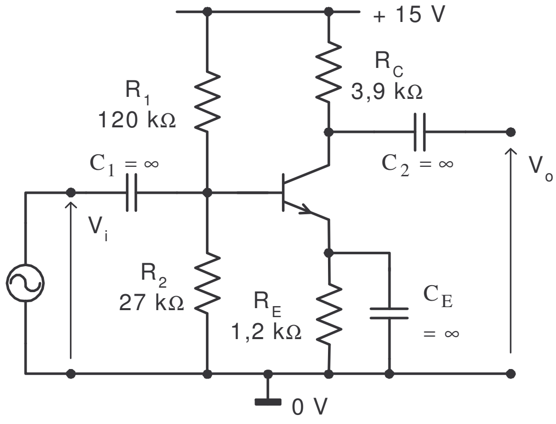

Figure 3

4.2 Briefly explain the main advantage of the biasing circuit in Fig. 1 and using the equation for I_E indicate what circuit conditions must be met for this advantage to be realized.

4.3 A student *attempts* to connect this circuit as a common emitter amplifier as shown above. She mistakenly omits to connect the emitter bypass capacitor C_E. Draw an ac small-signal equivalent circuit for this amplifier (without C_E) using an appropriate model for the BJT, assuming $V_T = 25$ mV and $V_A = \infty$. Hence determine the voltage gain $A_v = v_o / v_i$, input resistance R_i and output resistance R_o of the amplifier as she connected it.

4.4 If C_E had been connected, the voltage gain and input resistance would have been significantly different. Determine the voltage gain and input resistance of the amplifier with C_E connected.

4.5 If a load resistance R_L that is much less than R_C is now connected to this amplifier, the voltage gain will be significantly reduced. To minimize this effect, a common collector stage may be added as shown in Fig. 4 below.

1. Assuming $I_{B2} << I_{C1}$, determine the emitter current I_{E2} of Q_2.
2. A load resistance R_L of 600 Ω is now connected to the output of the amplifier. Assuming β for Q_2 is 100, determine the input resistance looking into the base of Q_2 with R_L connected, again assuming $V_T = 25$ mV and $V_A = \infty$.
3. Hence determine the overall voltage gain $A_v = v_o / v_i$ of the amplifier with R_L connected.

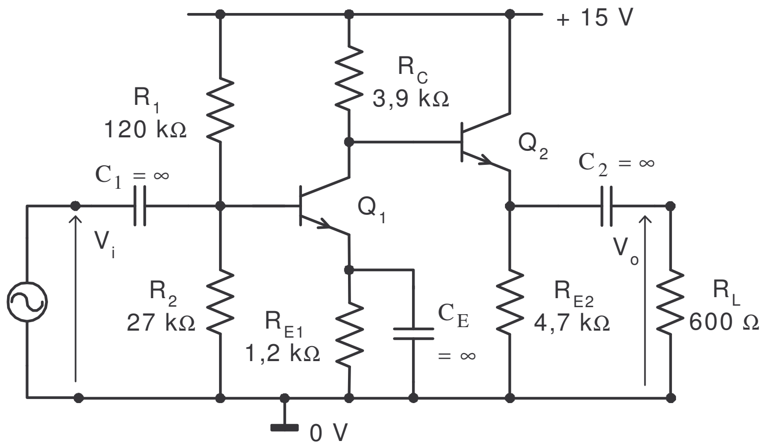

Figure 4